CLAIMS

1. A method for forming an electronic device in a multilayer structure comprising the steps of:

defining a topographic profile in a laterally extending first layer;

depositing at least one non-planarizing layer on top of the first layer such that the topographic profile of the surface of the or each non-planarizing layer conforms to that of the laterally extending first layer; and

depositing a pattern of at least one additional layer onto the top-most non-planarizing layer, such that the lateral location of the additional layer is defined by the shape of the topographic profile of the non-planarizing layer, and whereby the additional layer is laterally aligned with the topographic profile in the first layer.

2. A method as claimed in claim 1, wherein the additional layer is deposited from solution.

3. A method as claimed in claim 1 or 2, wherein prior to the step of depositing the additional layer, the method further comprises the step of performing a surface modification process that has a different effect on relatively raised regions of the non-planarizing layer in comparison to relatively depressed regions of the non-planarizing layer, so as to generate a surface energy contrast between the relatively raised and relatively depressed regions of the non-planarizing layer.

4. A method as claimed in claim 3, wherein the surface modification process comprises selectively depositing a surface modification material which modifies the surface energy of the substrate.

5. A method as claimed in any preceding claim, wherein the substrate comprises a flexible plastic substrate such as poly(ethleneterephtalate) (PET), polyethersulphone (PES) or polyethernaphtalene (PEN).

6. A method as claimed in claim 3 or 4, wherein the step of performing a surface modification process comprises laminating the surface of the substrate by bringing the surface into contact with a flat stamp bearing a surface modification material.

7. A method as claimed in claim 6, wherein the surface modification material is a self assembled monolayer (SAM).

8. A method as claimed in claim 6 and 7, wherein the SAM is able to bond to a functional group on the surface, and has a tail containing a polar group.

9. A method as claimed in any preceding claim, wherein the non-planarizing layers are deposited by vacuum deposition techniques.

10. A method as claimed in any preceding claim, wherein the non-planarizing layers are deposited from solution.

11. A method as claimed in claim 6, further comprising the step of applying a mechanical support layer to the surface of the non-planarizing layer in order to maintain separation of the flat stamp and relatively depressed regions of the non-planarizing layer during the step of performing a surface modification process.

12. A method as claimed in any preceding claim, wherein the topographic profile in the first layer is created by embossing the first layer.

13. A method as claimed in any preceding claim, wherein the method further comprises, prior to the step of depositing at least one non-planarizing layer, the step of depositing a solution of conductive or semiconductive material into at least one depressed region of the topographic profile in the first layer.

14. A method as claimed in claim 13, wherein said solution of conductive or semiconductive material partially fills at least one depressed region of the topographic profile in the first layer.

15. A method as claimed in claims 13 or 14, wherein prior to the step of depositing conductive or semiconductive material onto the topographic profile the method further comprises the step of performing a surface modification process that has a different effect on relatively raised regions of the first layer in comparison to relatively depressed regions of the first layer, so as to generate a surface energy contrast between the relatively raised and relatively depressed regions of the first layer.

16. A method as claimed in claims 13, 14 or 15, wherein the deposition of the conductive or semiconductive material onto the topographic profile inverts a surface energy contrast between a relatively raised region and the relatively depressed region of the topographic profile such that a region with a relatively high surface energy prior to the deposition step has a relatively low surface energy subsequent to the deposition step.

17. A method as claimed in any one of claims 13 to 16, wherein the conductive or semiconductive material deposited onto a region of the topographic profile in the first layer forms one or more functional elements of the electronic device.

18. A method as claimed in claim 17, wherein the one or more functional elements of the electronic device are electrodes of the electronic device.

19. A method as claimed in any preceding claim, wherein prior to the step of depositing at least one additional layer, the method further comprises the step of applying a surface modification layer on one of the relatively raised or relatively lowered regions of the top-most non-planarizing layer such that the additional layer is confined to the other of the relatively raised or relatively lowered regions of the top-most non-planarizing layer.

20. A method as claimed in claim 19, wherein prior to the step of applying a surface modification layer, a surface treatment step is applied selectively to one of the relatively raised or relatively lowered regions of the non-planarizing layer.

21. A method as claimed in claims 19 or 20, wherein the surface treatment step comprises a step in which the additional non-planarizing layer is made wetting for the deposition of the additional layer.

22. A method as claimed in any one of claims 19, 20 or 21, wherein the surface modification layer is a low surface energy polymer.

23. A method as claimed in claim 3 or any of claims 4 to 22 when dependent on claim 3, wherein the step of performing a surface modification process comprises depositing a surface modification material onto the substrate at an oblique angle such that the surface modifying material is deposited onto the raised portions of the substrate, and the depressed portions are shadowed by the raised portions during the deposition of the surface modification material.

24. A method as claimed in claim 23, wherein the low surface energy polymer is a fluoropolymer.

25. A method as claimed in any preceding claim, wherein the additional layer forms an electrically functional element of the electronic device.

26. A method as claimed in any of claims 19 to 24, wherein the surface energy of surface modification layer is modified according to a topographic profile of the surface modification layer.

27. A method as claimed in any of claims 1 to 12, wherein the method further comprises, prior to the step of depositing at least one non-planarizing layer, depositing conductive or semiconductive material onto at least one raised region of the topographic profile in the first layer.

28. A method as claimed in claim 27, wherein prior to the step of depositing conductive or semiconductive material onto the topographic profile the method further comprises the step of performing a surface modification process that has a different effect on relatively raised regions of the first layer in comparison to relatively depressed regions of the first layer, so as to generate a surface energy contrast between the relatively raised and relatively depressed regions of the first layer.

29. A method as claimed in claim 27 or 28, wherein the deposition of the conductive or semiconductive material onto the topographic profile inverts a surface energy contrast between the relatively raised region and a relatively depressed region of the topographic profile.

30. A method as claimed in claim 27, wherein the conductive or semiconductive material deposited onto a region of the topographic profile in the first layer forms one or more electrodes of the electronic device.

31. A method as claimed in any of claims 1 to 11, wherein the step of defining a topographic profile comprises the deposition of conductive or semiconductive material onto a first layer.

32. A method as claimed in any of claims 16 to 31, wherein the conductive or semiconductive material deposited onto the first layer comprises a functional element of the electronic device.

33. A method as claimed in claim 32, wherein the functional element is a gate electrode of the electronic device.

34. A method as claimed in any preceding claim, wherein the pattern of the at least one additional layer deposited onto the non-planarizing layer comprises at least one functional element of the electronic device.

35. A method as claimed in claim 34, wherein the at least one functional element comprises a source and a drain electrode of the electronic device.

36. A method as claimed in claim 32, wherein the at least one functional element comprises a source and a drain electrode of the electronic device.

37. A method as claimed in any of claims 1 to 31, wherein the pattern of the at least one additional layer deposited onto the non-planarizing layer comprises a functional element of the electronic device.

38. A method as claimed in claim 37, wherein the functional element is a gate electrode of the electronic device.

39. A method as claimed in any preceding claim, wherein the electronic device is a transistor.

40. A method as claimed in any preceding claim, wherein the step of depositing at least one non-planarizing layer comprises depositing a first non-planarizing layer and a second non-planarizing layer.

41. A method as claimed in claim 40, wherein the first non-planarizing layer is a semiconductor layer.

42. A method as claimed in claim 40 or 41, wherein the second non-planarizing layer is a dielectric layer.

43. A method as claimed in claim 42, wherein the dielectric layer is a gate dielectric layer.

44. A method as claimed in any preceding claim, wherein the additional layer is laterally aligned with the topographic profile in the first layer such that a lateral overlap between edges of the additional layer and boundaries of the topographic profile in the first layer to which the additional layer is confined is less than 10 μm.

45. A method as claimed in any preceding claim, wherein the additional layer is laterally aligned with the topographic profile in the first layer such that a lateral overlap between edges of the additional layer and boundaries of the topographic profile in the first layer to which the additional layer is confined is less than 5 μm.

46. A method as claimed in any preceding claim, wherein the additional layer is laterally aligned with the topographic profile in the first layer such that a lateral overlap between edges of the additional layer and boundaries of the topographic profile in the first layer to which the additional layer is confined is less than 1 μm.

substrate in a solvent in which the sacrificial layer is soluble, but in which the surface layer is insoluble.

47. A method as claimed in claim 3 or any of claims 4 to 46 when dependent on claim 3, wherein the step of performing a surface modification process on a surface having a topographic profile comprising at least one relatively raised region and at least one relatively depressed region, comprises:

depositing a planarizing sacrificial layer over the topographic profile;

etching the surface of the sacrificial layer to reveal the relatively raised regions of the surface, but leaving the relatively depressed regions covered by the sacrificial layer, so as to define a layer having a substantially planar upper surface;

performing a surface energy modification process on the surface layer; and

removing the remaining areas of the sacrificial layer to reveal the depressed regions.

48. A method as claimed in claim 47, wherein the planarizing sacrificial layer is deposited by spin coating.

49. A method as claimed in claim 47 or 48, wherein the planarizing sacrificial layer is deposited by a polymer solution.

50. A method as claimed in claim 49, wherein the polymer solution is an organic based polymer solution containing siloxane.

51. A method as claimed in any of claims 47 to 50, wherein the etching step comprises an oxygen plasma etching step.

52. A method as claimed in any of claims 47 to 51, wherein the step of performing a surface energy modification process on the surface layer, comprises exposing the surface layer to a vapour of a self-assembling molecule.

53. A method as claimed in any of claims 47 to 52, wherein the step of removing the remaining areas of the sacrificial layer comprises washing the